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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/661,281	09/14/2000	Noboru Mohri	43890-439	6246
7590 08/01/2005 McDermott Will & Wmery 600 13th Street NW Washington, DC 20005-3096			EXAMINER PATEL, ISHWARBHAI B	
			ART UNIT 2841	PAPER NUMBER

DATE MAILED: 08/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/661,281

Applicant(s)

MOHRI ET AL

Examiner

Ishwar (I. B.) Patel

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 05 July 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 22-24 and 26-31 is/are pending in the application.
- 4a) Of the above claim(s) 23, 24 and 27-31 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 22 and 26 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 May 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☒ Certified copies of the priority documents have been received in Application No. 09/041,666.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>1/10/05</u>   | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Divisional***

1. This application is divisional of Application Number 09/041, 666, filed on March 13, 1998, Patent No. 6,132, 543. The examiner has reviewed the prior art used in the parent application. MPEP 2001.06(b).

### ***Election/Restrictions***

2. Applicant's election of Specie IV, reading on figure 9, claims 22 and 26, in the reply filed on July 5, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

### ***Specification***

3. The abstract of the disclosure is objected to because the abstract is in two paragraphs. The abstract should be in narrative form and generally limited to a single paragraph on separate sheet within the range of 50 to 159 words. Correction is required. See MPEP § 608.01(b).

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 22 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamzehdoost et al., US Patent No. 5,689,091 (Hamzehdoost), in view of Muyschondt et al., US Patent No. 5,646,368 (Muyschondt).

**Regarding claim 22**, Hamzehdoost, in figure 4 and 5, discloses packaging substrate comprising: a circuit substrate (14, shown in detail in figure 2a), a first conductor pattern formed onto said circuit substrate (patterns on upper surface of the substrate 14, column 3, line 29-31), a second conductor pattern (patterns on lower surface of the substrate 14, column 3, line 29-31), electrically connected to said first conductor pattern on the opposite side of the circuit substrate via through holes (18a,18b, shown in detail in figure 1c), and a first ball-shaped solder (44) joined to said second conductor patterns (see figure 4 and 5).

Hamzehdoost does not disclose a surface roughness of the circuit substrate made larger on a printing surface of the second conductor pattern than on a printing surface of the first conductor pattern.

Muyschondt discloses a circuit board and recites that one circuit pattern can be formed on a copper laminated insulated sheet and the other on a build up layer can be formed by surface laminating the insulating layer on top of the other with the surface of the insulating layer roughened to provide a capability of adhering copper to that surface. This implies that the surface insulation layer with copper lamination does not need any roughening, but the surface on which the patterns are formed by plating needs the roughened surface. In other words, the roughness of the surface on one side is greater

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than that on the other side, depending upon the method of manufacturing the circuit board. Also, as the circuit pattern on the other side is made by plating the copper layer, a thinner layer can be plated, resulting in the saving of the copper lost in etching.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicants invention to provide the circuit board of Hamzehdoost with a surface roughness of the circuit substrate made larger on a printing surface of the second conductor pattern than on a printing surface of the first conductor pattern, as taught by Muyshondt, in order to reduce the loss of copper lost in etching and the surface roughened to have desired adherence of the plating.

Regarding the limitation "a first conductor pattern formed by an intaglio printing means on flexible resin base material and transferred onto said circuit substrate", it is the process limitation in a product claims. Such a process limitation defines the claimed invention over the prior art only to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art, in the case that the product is the same as, or obvious over, the prior art. See *Product – by – Process* in MPEP § 2113 and 2173.05(p) and *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985). Therefore, the modified circuit board of Hamzehdoost meets the limitation.

**Regarding claim 26**, the modified circuit board of Hamzehdoost further discloses a dielectric layer (24a or 24b, figure 2b) formed on a portion of the first conductor pattern or said second conductor pattern and a third conductor pattern (34 or 36 respectively) formed on top of said dielectric layer (see figure 4 and 5).

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Enomoto, US Patent No. 4,715,117, in figure 2(H) discloses a ceramic wiring board with fine pattern formed on the roughened surfaces, column 5, line 22 to 55.

Yamaguchi, US Patent No. 5,886,876, in figure 2(c) discloses a circuit board with conductor pattern (14) on first side and conductor patterns (15) on opposite of the circuit substrate (11) with a ball shape terminal connected to the conductor pattern (15).

Wang et al., US Patent No. 5,519,177 discloses roughened surface for electroless plating, column 1, line 21-26.

Yamaguchi et al., US Patent No. 5,763,059, in figure 1, discloses ceramic substrate (1) with patterns on both the surfaces and a solder ball (4) connected to the patterns on the bottom surface.

Freyman et al. US Patent No. 4,700,473, in figure 6, discloses a ceramic substrate (200) with conductive pattern (210) on one surface and (204) on the other surface with solder plug (206) connected to the other patterns (204).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Ishwar (I. B.) Patel  
Examiner

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July 21, 2005